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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,990	02/11/2004	Back-Won Lee	21C-0113	8230

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EXAMINER	
TANG, MINH NHUT	
ART UNIT	**PAPER NUMBER**
2829	

DATE MAILED: 10/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

CTL

Office Action Summary	Application No.	Applicant(s)	
	10/777,990	LEE, BACK-WON	
	Examiner	Art Unit	
	Minh N. Tang	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 6-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6,7 and 9-23* is/are rejected.

7)☒ Claim(s) *8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 February 2004 and 04 August 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings were received on August 04, 2005. These drawings are accepted.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 10-17, and 21-23 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

In claim 10, lines 7-8, the limitation "the driving part has a plurality of first switching devices formed on the lower substrate" is not supported by the original specification. Applicant, in the Remarks page 10, asserted that support for amended claim 10 can at least be found in original filed Figures 9 and 10a-10c; however, the examiner could not find any support for the limitation above.

In claim 21, lines 1-4, the limitation "the driving part has a plurality of first switching devices formed on the lower substrate via a thin film process, and the pixel part has a plurality of second switching devices formed on the lower substrate via the thin film process" is not supported by the original specification.

In claim 23, lines 1-3, the limitation "the driving part has a plurality of first amorphous silicon transistors formed on the lower substrate, and the pixel part has a plurality of second amorphous silicon transistors" is not supported by the original specification.

Claims 11-17 and 22 are rejected since they depend on rejected base claims.

Claim Objections

4. Claims 12, 21 are objected to because of the following informalities:

a/ in claim 12, line 1, "an end portions" should be -- end portions --.

b/ in claim 21, line 2, there is an insufficient antecedent basis for the limitation "the lower substrate". For examination purposes, "the lower substrate" is interpreted as -- a lower substrate of the mother substrate --.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-4, 6-7, 9 and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Shimada et al. (U.S.P. 5,576,730).

As to claim 1, Shimada et al. disclose, in Fig. 7, a mother substrate (22) comprising: a plurality of display cells (i.e., rows defined by a plurality of gate lines 1, hereinafter cells), each of the display cells (cells) having an inspection line (i.e.,

leftmost/uppermost lines connecting to the gate/source driving circuits 5, 6, hereinafter connecting lines) receiving a first inspection signal (GND, VDD, CLK, START) externally provided (see column 6, lines 54-58), a driving part (5, 6) outputting a second inspection signal (Y1, Y2, ..., Yn; X1, X2, ..., Xn) in response to the first inspection signal (GND, VDD, CLK, START) provided through the inspection line (connecting lines), and a pixel part (i.e., defined by boundary gate line 1 and data line 2) being driven in response to the second inspection signal (Y1-Yn, X1-Xn); and an inspecting pad part (see the ends of the connecting lines, hereinafter, pads) extended from the inspection line (connecting lines) so as to provide the first inspection signal (GND, VDD, CLK, START) to the inspection line (connecting lines), wherein the inspection line (connecting lines) comprises: a plurality of input lines (i.e., right/lower part of the connecting lines) connected to the driving part (5, 6) and spaced apart from each other in a predetermined distance; and a connecting line (A) electrically connected between the input lines (right/lower part of the connecting lines), and electrically connected between the input lines (right/lower part of the connecting lines) and the inspecting pad part (pads).

As to claim 2, Shimada et al. disclose in Fig. 7, the pixel part (defined by boundary gate line 1 and data line 2) comprises a plurality of pixels (i.e., defined by two adjacent gate lines 1 and data lines 2), each of the pixels having a gate line (1), a data line (2) substantially perpendicular to the gate line (1) and a switching device (4) connected to the gate and data lines (1, 2).

As to claim 3, Shimada et al. disclose in column 6, lines 54-58, and column 7,

lines 51-55, the driving part (5, 6) comprises a shift register having a plurality of stages (i.e., for sequentially sending signals Y1-Yn, X1-Xn) so as to output the second inspection signal (Y1-Yn, X1-Xn) to the gate line (1).

As to claim 4, Shimada et al. disclose in Fig. 7, the first inspection signal (GND, VDD, CLK, START) has a voltage level (GND, VDD) suitable for substantially simultaneously driving the stages.

As to claim 6, Shimada et al. disclose in Fig. 7, the input lines (right/lower part of the connecting lines) comprise a start signal input line (i.e., line connecting to START signal), a clock input line (i.e., line connecting to CLK signal) and a driving voltage input line (i.e., lines connecting to GND, VDD signals) so as to receive signals used to drive the driving part (5, 6).

As to claim 7, Shimada et al. disclose in Fig. 7, the start signal input line (line connecting to START signal) is connected to a first stage of the stages.

As to claim 9, Shimada et al. disclose in Fig. 7, the driving voltage input line (lines connecting to GND, VDD signals) receives a ground voltage (GND).

As to claim 21, Shimada et al. disclose in Fig. 7, the driving part (6) has a plurality of first switching devices (7) formed on a lower substrate of the mother substrate (22) via a thin film process, and the pixel part has a plurality of second switching devices (4) formed on the lower substrate via the thin film process

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 10-20 and 23 are rejected under 35 U.S.C. 102(e) as being anticipated by Kim (U.S.P. 6,781,403).

As to claim 10, Kim discloses, in Figs. 1 and 2, a substrate (1) for a display panel, comprising: a lower substrate (2) having an inspection line (26) receiving a first inspection signal (i.e., gate driving signals) externally provided (see column 1, lines 64-67 and column 2, lines 61-64), a driving part (16) outputting a second inspection signal (i.e., scanning signal) in response to the first inspection signal (gate driving signals) provided through the inspection line (26), and a pixel part (i.e., defined by boundary gate lines 20 and data lines 18) being driven in response to the second inspection signal (scanning signal); and an upper substrate (4) being coupled to the lower substrate (2), wherein the pixel part (boundary gate lines 20 and data lines 18) has a plurality of second switching devices (i.e., thin film transistors) formed on the lower substrate (2).

As to claim 11, Kim discloses in Fig. 1, the inspection line (26) comprises a plurality of input lines (28) spaced apart from each other in a predetermined distance; and a connecting line (22) electrically connected between the input lines (28).

As to claim 12, Kim discloses in Fig. 1, end portions of the input lines (28) are disposed on an edge portion of the lower substrate (2), and a connection line (i.e., part of the input lines 28) electrically connected between the end portions of the input lines

(28) is disposed on the edge portion of the lower substrate (2).

As to claim 13, Kim discloses in Fig. 1, the lower substrate (2) is partially grinded (i.e., after the inspection is complete), the end portions of the input lines (28) disposed on the edge portion and a portion of the connecting line (22) disposed on the edge portion are removed while the lower substrate (2) is grinded (i.e., outer edge of the lower substrate 2 is cut for providing a display device).

As to claim 14, Kim discloses in Fig. 2, the input lines (28) comprise a start signal input line (for providing a gate start pulse GSP), a clock input line (for providing a gate shift clock signal GSC) and a driving voltage input line (for providing voltage signals Vcom, VGL, GND).

As to claim 15, Kim discloses in Fig. 2, the driving voltage input line (for providing voltage signals Vcom, VGL, GND) has a width wider than those of the start signal input line (for providing a gate start pulse GSP) and clock input line (for providing a gate shift clock signal GSC).

As to claim 16, Kim discloses in Figs. 1 and 2, the driving voltage input line (for providing voltage signals Vcom, VGL, GND) receives a first inspection signal (gate driving signal) externally provided, and provides the first inspection signal (gate driving signal) to the inspection line (26).

As to claim 17, Kim discloses in column 2, lines 37-41, a liquid crystal layer disposed between the lower substrate (2) and the upper substrate (4).

As to claim 18, Kim discloses, in Figs. 1 and 2, a method of manufacturing a display panel (21), comprising: fabricating a substrate (1) for a display panel (21), the

substrate (1) having a lower substrate (2) and an upper substrate (4) coupled to the lower substrate (2), the lower substrate (2) having an inspection line (26) receiving a first inspection signal (gate driving signal) externally provided, a driving part (16) outputting a second inspection signal (scanning signal) in response to the first inspection signal (gate driving signal) provided through the inspection line (26), and a pixel part (21) being driven in response to the second inspection signal (scanning signal); providing the first inspection signal (gate driving signal) to the inspection line (26) to inspect the driving part (16) and pixel part (21); and insulating the inspection line (26) from an input line (28) to complete the display panel (21), wherein the driving part (16) and the pixel part (21) are formed on the lower substrate (2).

As to claim 19, Kim discloses in Fig. 1, fabricating a mother substrate (2) for the lower substrate (2) having an inspecting pad part extended from the inspection line (26); providing the first inspection signal (gate driving signal) to the inspecting pad part to inspect the mother substrate (2) for the lower substrate (2); fabricating a mother substrate (4) for the upper substrate (4); combining the mother substrate for the lower substrate (2) with the mother substrate for the upper substrate (4); and cutting the combined substrate to complete the substrate for the display panel (21).

As to claim 20, Kim discloses in Fig. 1, the inspection line (26) is removed by grinding (i.e., cut to form a display device) an edge of the substrate for the display panel (21).

As to claim 23, as best understood, Kim discloses in Fig. 1, the pixel part (21) has a plurality of transistors (i.e., thin film transistors).

Allowable Subject Matter

9. Claims 8 and 22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

10. Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) of rejection.

Applicant, in the Remarks page 13 filed on August 04, 2005, asserted that the signals to the inspection line are not externally provided. The examiner respectfully disagrees because, as admitted by the Applicant, the signals from the timing controller and power supply go through the data PCB 12, the gate driving signal transmission group 22, through the LOG-type signal line group 26, finally to gate driver IC 16; therefore the signals applied to the signal line group 26 from the timing controller and power supply that is are clearly externally provided. Furthermore, as disclosed in column 1, line 57 to column 2, line 9, of the Kim reference, the control signals and direct current voltage signals inputted from the exterior over signals lines mounted onto a printed circuit board connected to the TCP.

Applicant, on page 13 of the Remarks, also asserted that the gate driver IC mounted on the TCP 14, not the lower substrate as recited in amended claims 10 and 18. The examiner respectfully disagrees since, as disclosed in column 1, lines 59-63 and column 2, lines 10-15 of the Kim reference, each date drive IC and gate drive IC are mounted in a tape carrier package (TCP) for connection to the liquid crystal display

panel by a tape automated bonding (TAP) system, or mounted onto the liquid crystal display panel by a chip on glass (COG) system, the drive ICs mounted onto the liquid crystal display panel by the COG system at a lower glass; therefore it is believed that the gate driver IC could be mounted on the TCP or alternately mounted onto the lower substrate.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Communication

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh N. Tang whose telephone number is (571) 272-1971. The examiner can normally be reached on M-F (7:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nestor R. Ramirez can be reached on (571) 272-2034. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Minh Tang

MINH NHUT TANG
PRIMARY EXAMINER

10/13/05